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SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
ARCOS, CAROLINE H	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,587	KLAUSLER, PETER M.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-10,13-18 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-10,13-18 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/06/2008 and 01/25/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 5-10, 13-18 and 21-24 are pending for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-2, 5-10, 13-18 and 21-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claim language in the following claims is not clearly understood:

i. As per claim 1, it is unclear what are the criteria for the occurrence of the context shifting event? (i.e. failure, load balancing or interrupt?) line 10, it is unclear what is the criteria for migrating one of the plurality of the program units and what are the criteria to migrate more of the plurality of the program unit? And what are the conditions for the selection of the one of the plurality of multiple processing units to which the program units are migrated. (i.e. is it any one of the plurality of processor unit or the one that has most of the program units associated with one process?) Line 12, the claim recites the limitation "such that, the plurality of program units associated with the process are executing on the same multiple processor unit. This limitation is interpreted as the intended result of migration based the on the occurrence of the context shifting event. In addition line 15, the claim recites "such that" each of the plurality of program units process

the same context shifting event as the first program unit. Claim scope is not limited by claim language that suggests or make optional but does not require steps to be performed, or by claim language that doesn't limit a claim to a particular structure. See MPEP 2111.04. If it is applicant's intention to limit the scope of the claim with these limitations, applicant should rewrite the limitation to positively recite the features of the limitations identified above.

ii. As per claim 9, it has the same deficiency as claim 1.

iii. As per claim 17, it has the same deficiency as claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5-10, 13-18 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shaylor (US2004/0117793 A1), in view of Gillespie (US 6,269,391 B1) and further in view of Koenen (US 2004/0019891 A1).

6. As per claim 1, Shaylor teaches the invention substantially as claimed including a method for scheduling a plurality of program units, the method comprising:

starting a process within an operating system executing in a system having a plurality of multiple processor units, starting the plurality of program units within the operating system, the

plurality of program units associated with the process (par. [0010]; par. [0026], lines 13-18; par. [0027]; par. [0031]), wherein the plurality of program units execute on two or more of the plurality of multiple processor units (par. [0079], lines 1-7; par. [0081]); and

upon the occurrence of a context shifting event for a first program unit of the plurality of program units, performing the tasks of:

migrating one or more the plurality of program units from one or more of the plurality of multiple processing units to one of the plurality of multiple processing units such that the plurality of program units associated with the process are executing on the same multiple processor unit and such that each of the plurality of program units process the same context shifting event as the first program unit (par. [0010]; par. [0082], lines 10-17; par. [0084]).

Synchronizing the scheduling of each of the plurality of program units (par. [0032]; (par. [0034]; par. [0086]).

7. Shaylor doesn't explicitly teach each of the multiple processor units having a plurality of processors and setting the context of each of the plurality of program units (par. [0055]).

8. However, Gillespie teaches setting the context of each of the plurality of program units such that each of the plurality of program units process the same context shifting event as the first program unit (col. 3, lines 45-53; wherein "thread – control object" is the context of each of the plurality of program units as claimed).

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor and Gillespie because Gillespie's teaching of synchronizing execution and setting context of each of the plurality of program units would improve system performance by saving the context / state of each of the plurality of program units prevents redundant data execution and prepare the threads for continuing execution from the point they were stopped.

10. The combined teaching of Shaylor and Gillespie doesn't explicitly teach that each of the multiple processor units having a plurality of processors. However, Koenen teaches each of the multiple processor units having a plurality of processors (abs.; par. [0045]).

11. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor, Gillespie and Koenen because Koenen teaching of having multiple processors with multi cores would improve the system by replacing each of the plurality of the processors with one of the multi core processor which improve system performance and throughput.

12. As per claim 2, Shaylor teaches that the program unit comprises a thread (par. [0010]; par. [0026]; par. [0027]; par. [0081]).

13. As per claim 5, Gillespie teaches that the context shifting event comprises an exception (col. 4, lines 26-27).

14. As per claim 6, Gillespie teaches the exception comprises a signal (col. 4, lines 26-27; col. 5, lines 58-59).

15. As per claim 7, Gillespie teaches the context shifting event comprises a non-local goto (col. 18, lines 40-45).

16. As per claim 8, Shaylor teaches the context shifting event comprises a system call (par. [0014]; par. [0026]; par. [0055]).

17. As per claim 9, Shaylor teaches a system for scheduling a plurality of program units, the system comprising:

a plurality of multiple processor units (par. [0010]; par. [0081]; par. [0088]),

a memory coupled to the plurality of multiple processor units (par. [0040]); and

start a process, start the plurality of program units within an operating system, the plurality of program units associated with the process(par. [0010]; par. [0026], lines 13-18; par. [0027]; par. [0031]), wherein the plurality of program units execute on two or more of the plurality of multiple processor units (par. [0079], lines 1-7; par. [0081]); and

upon the occurrence of a context shifting event for a first program unit of the plurality of program units, at least one of the processors performs the tasks

of:

migrate one or more of the plurality of program units from one or more of the plurality of multiple processing units to one of the plurality of multiple processing units such that the plurality of program units associated with the process are executing on the same multiple processor unit (par. [0010]; par. [0082], lines 10-17; par. [0084]),

synchronize the scheduling of each of the plurality of program units, and such that the plurality of program units process the same context shifting event as the first program unit (par. [0032]; (par. [0034]; par. [0086]).

18. Shaylor doesn't explicitly teach that each multiple processor unit having a plurality of processors, an operating environment stored in the memory and executed by at least one of the processors ; wherein each of the plurality of processors on a multiple processor unit shares cache memory; set the context of each of the plurality of program units.

19. However, Gillespie teaches an operating environment stored in the memory and executed by at least one of the processors (col. 14, lines 35-56) and setting the context of each of the plurality of program units.(col. 3, lines 45-53; wherein "thread – control object" is the context of each of the plurality of program units as claimed).

20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor and Gillespie because Gillespie's teaching of synchronizing execution and setting context of each of the plurality of program units would improve system

performance by saving the context / state of each of the plurality of program units prevents redundant data execution and prepare the threads for continuing execution from the point they were stopped.

21. The combined teaching of Shaylor and Gillespie doesn't explicitly teach that each multiple processor unit having a plurality of processors, wherein each of the plurality of processors on a multiple processor unit shares cache memory. However, Koenen teaches each multiple processor unit having a plurality of processors, wherein each of the plurality of processors on a multiple processor unit shares cache memory (abs.; par. [0045]).

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor, Gillespie and Koenen because Koenen teaching of having multiple processors with multi cores would improve the system by replacing each of the plurality of the processors with one of the multi core processor which improve system performance and throughput.

23. As per claim 10, Shaylor teaches the program unit comprises a thread (par. [0010]; par. [0026]; par. [0027]; par. [0081]).

24. As per claim 13, t Gillespie teaches that the context shifting event comprises an exception (col. 4, lines 26-27).

25. As per claim 14, Gillespie teaches the exception comprises a signal (col. 4, lines 26-27; col. 5, lines 58-59).

26. As per claim 15, Gillespie teaches the context shifting event comprises a non-local goto (col. 18, lines 40-45).

27. As per claim 16, Shaylor teaches the context shifting event comprises a system call (par. [0014]; par. [0026]; par. [0055]).

28. As per claim 17, it is the computer storage medium of the method claim 1. Therefore, it is rejected under the same rational.

29. As per claim 18, it is the computer storage medium of the method claim 2. Therefore, it is rejected under the same rational.

30. As per claim 21, it is the computer storage medium of the method claim 5. Therefore, it is rejected under the same rational.

31. As per claim 22, it is the computer storage medium of the method claim 6. Therefore, it is rejected under the same rational.

32. As per claim 23, it is the computer storage medium of the method claim 7. Therefore, it is rejected under the same rational.

33. As per claim 24, it is the computer storage medium of the method claim 8. Therefore, it is rejected under the same rational.

Response to Arguments

34. Applicant's arguments with respect to claims 1-2, 5-10, 13-18 and 21-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 20040216113 A1 teaches Accounting method and logic for determining per-thread processor resource utilization in a simultaneous multi-threaded (SMT) processor.

US 5825649 A teaches Kernel substitution method in multi-processor system and multi-processor system having kernel substitution function.

US 6189111 B1 teaches Resource harvesting in scalable, fault tolerant, single system image clusters.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151.

The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VAN H NGUYEN/
Primary Examiner, Art Unit 2194

/Caroline Arcos/
Examiner, Art Unit 2195